

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S):

Fitzgerald et al.

SERIAL NO.:

10/625,018

GROUP NO.:

Not Yet Assigned

FILING DATE:

July 23, 2003

EXAMINER:

Not Yet Assigned

TITLE:

CMOS Inverter and Integrated Circuits Utilizing Strained Silicon

Surface Channel MOSFETs

CERTIFICATE OF FIRST CLASS MAILING UNDER 37 C.F.R. 1.8

I hereby certify that this correspondence, and any document(s) referred to as enclosed herein, is/are being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 2 day of December, 2003.

Emy Walsh

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

Submitted herewith are:

- 1. Transmittal Form (1 pg.);
- 2. Supplemental Information Disclosure Statement (2 pgs.);
- 3. Form PTO-1449 (13 pgs.);
- 4. Copies of cited references B1-B38 and C1-C91; and
- 5. Return Receipt Postcard.

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		Filing Date		July 23	3, 2003		
DEC 3 1 2003		First Named I	Inventor	Fitzger	rald		
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FORM		Attorney Doc	ket No.	ASC-0	043C2		
		Patent No.		Not A	pplicable		
		Issue Date		Not A	pplicable		
	ENC	LOSURES (ch	eck all that apply)				
Fee Transmittal Form		Copy of Notice	to File Missing		Notice of Appeal to Board of Patent Appeals and Interferences		
Check Attached		Parts of Applica	ation				
Copy of Fee Transmittal Form		Formal Drawin	g(s)		Appeal Brief (in triplicate)		
Amendment/Response		Request For Co			Status Inquiry		
☐ Preliminary ☐ After Final]	Transmittal		\boxtimes	Return Receipt Postcard		
Affidavits/declaration(s) Letter to Official Draftsperson			Power of Attorney (Revocation of Prior Powers)		Certificate of First Class Mailing under 37 C.F.R. 1.8		
including Drawings [Total Sheets]		Terminal Disclaimer			Certificate of Facsimile Transmission under 37 C.F.R. 1.8		
Petition for Extension of Time		Executed Declaration and Power of Attorney for Utility or Design Patent Application			Additional Enclosure(s) (please identify below)		
Supplemental Information Disclosure Statement		Small Entity St	tatement				
Form PTO-1449 Copies of IDS Citations (B1-B38 and C1-C91)		CD(s) for large program	e table or computer				
Certified Copy of Priority		Amendment A	fter Allowance				
Document(s) Sequence Listing submission Paper Copy/CD Computer Readable Copy Statement verifying identity of above		Correction	Certificate of Correction (in				
CORRESPONDENCE ADDRESS			SIGNATURE BL	оск	Danie (C.H. 1 1 1 1 1		
Direct all correspondence to: Patent Ad Testa, Hi High Structure 125 High Boston, I Tel. No.: Fax No.:	nibeault, LLP	Date: December 2/ Reg. No. 50,773 Tel. No.: (617) 248 Fax No.: (617) 248	Respectfully submitted, Mark L. Beloberodov Attorney for Applicants Testa, Hurwitz & Thibeault, LLP High Street Tower 125 High Street Boston, MA 02110				



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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

In accordance with the provisions of 37 C.F.R. 1.97 and 1.98, Applicants hereby make of record the patents and publications listed on the accompanying Form PTO-1449, and other information contained herein, for consideration by the Examiner in connection with the examination of the above-identified patent application. In accordance with the U.S. Patent Office's partial waiver of the requirement under 37 C.F.R. 1.98 (a)(2)(i), only copies of the foreign patent documents and non-patent publications are enclosed.

It is respectfully requested that each of the patents and publications listed on the attached Form PTO-1449, and other information contained herein, be made of record in this application.

In addition, Applicants wish to inform the Examiner about the following commonlyowned, co-pending patent applications, including all cited references and Office actions issued therein:

U.S. Serial Number	Filing Date	Inventor Name
09/599,260	06/22/2000	Wu et al.
09/764,177	01/17/2001	Fitzgerald
09/906,545	07/16/2001	Fitzgerald
10/216,085	08/09/2002	Fitzgerald
10/264,935	10/04/2002	Lochtefeld et al.

Information Disclosure Statement Serial No. 10/625,018 Page 2 of 2

In accordance with the provisions of 37 C.F.R. 1.97, this statement is being filed before the mailing of the first Office action on the merits. Applicants believe no fees are due for this paper to be entered and considered, but the Commissioner is hereby authorized to charge Deposit Account No. 20-0531 for any required fees that may be due.

Date: December <u>27</u>, 2003 Reg. No. 50,773

Tel. No.: (617) 248-7453 Fax No.: (617) 248-7100

2729959

Respectfully submitted,

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U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	Al	4,010,045	03/01/1977	Ruehrwein			
	A2	4,710,788	12/01/1987	Dämbkes et al.			
-	A3	4,990,979	02/05/1991	Otto			
	A4	4,997,776	03/05/1991	Harame et al.			
-	A5	5,013,681	05/07/1991	Godbey et al.			
,	A6	5,155,571	10/13/1992	Wang et al.			
	A7	5,166,084	11/24/1992	Pfiester			
	A8	5,177,583	01/05/1993	Endo et al.			
	A9	5,202,284	04/13/1993	Kamins et al.			
<u></u>	A10	5,207,864	05/04/1993	Bhat et al.			
	A11	5,208,182	05/04/1993	Narayan et al.			
	A12	5,212,110	05/18/1993	Pfiester et al.			
	A13	5,221,413	06/22/1993	Brasen et al.			
	A14	5,241,197	08/31/1993	Murakami et al.			
	A15	5,250,445	10/05/1993	Bean et al.			
	A16	5,285,086	02/08/1994	Fitzgerald			_
	A17	5,291,439	03/01/1994	Kauffmann et al.			
	A18	5,298,452	03/29/1994	Meyerson			
	A19	5,310,451	05/10/1994	Tejwani et al.			
	A20	5,316,958	05/31/1994	Meyerson			
	A21	5,346,848	09/13/1994	Grupen-Shemansky et al.			
	A22	5,374,564	12/20/1994	Bruel			
	A23	5,399,522	03/21/1995	Ohori			
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EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A24	5,413,679	05/09/1995	Godbey			
	A25	5,426,069	06/20/1995	Selvakumar et al.			
	A26	5,426,316	06/20/1995	Mohammad			
	A27	5,442,205	08/15/1995	Brasen et al.			
	A28	5,461,243	10/24/1995	Ek et al.	-		
	A29	5,461,250	10/24/1995	Burghartz et al.			
	A30	5,462,883	10/31/1995	Dennard et al.			
	A31	5,476,813	12/19/1995	Naruse			
	A32	5,479,033	12/26/1995	Baca et al.			
	A33	5,484,664	01/16/1996	Kitahara et al.			
	A34	5,523,243	06/04/1996	Mohammad			
	A35	5,523,592	06/04/1996	Nakagawa et al.			
	A36	5,534,713	07/09/1996	Ismail et al.			
	A37	5,536,361	07/16/1996	Kondo et al.			
	A38	5,540,785	07/30/1996	Dennard et al.			
	A39	5,596,527	01/21/1997	Tomioka et al.			
	A40	5,617,351	04/01/1997	Bertin et al.			
	A41	5,630,905	05/20/1997	Lynch et al.			
	A42	5,659,187	08/19/1997	Legoues et al.			
	A43	5,683,934	11/04/1997	Candelaria	-		
·	A44	5,698,869	12/16/1997	Yoshimi et al.			
	A45	5,714,777	02/03/1998	Ismail et al.			
	A46	5,728,623	03/17/1998	Mori			
	A47	5,739,567	04/14/1998	Wong			
EXAMIN	IER			DATE CONSI	IDERED	<u> </u>	



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U.S. PATENT DOCUMENTS SUB DOCUMENT DATE NAME **CLASS** FILING DATE IF EXAM. **CLASS** APPROPRIATE INIT. NUMBER 06/02/1998 Ek et al. 5,759,898 A48 07/28/1998 Otani et al. 5,786,612 A49 Nakato A50 5,792,679 08/11/1998 5,808,344 09/15/1998 Ismail et al. A51 5,847,419 12/08/1998 Imai et al. A52 03/02/1999 Goesele et al. 5,877,070 A53 5,891,769 04/06/1999 Liaw et al. A54 5,906,708 05/25/1999 Robinson et al. A55 5,912,479 06/15/1999 Mori et al. A56 5,943,560 08/24/1999 Chang et al. A57 10/05/1999 Chu et al. 5,963,817 A58 A59 5,966,622 10/12/1999 Levine et al. 5,998,807 12/07/1999 Lustig et al. A60 6,033,974 03/07/2000 Henley et al. A61 6,033,995 03/07/2000 Muller. A62 6,058,044 05/02/2000 Sugiura et al. A63 6,074,919 06/13/2000 Gardner et al. A64 08/01/2000 Chan et al. 6,096,590 A65 Gardner et al. 6,103,559 08/15/2000 A66 6,107,653 08/22/2000 Fitzgerald A67 6,117,750 09/12/2000 Bensahel et al. A68 10/10/2000 Mei et al. 6,130,453 A69 Favors et al. 6,133,799 10/17/2000 A70 6,140,687 10/31/2000 Shimomura et al. A71 **DATE CONSIDERED EXAMINER**



INFORMATION DISCLOSURE STATEMENT

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U.S. PATENT DOCUMENTS EXAM. DOCUMENT DATE NAME CLASS **SUB** FILING DATE IF INIT. NUMBER APPROPRIATE **CLASS** 11/07/2000 A72 6,143,636 Forbes et al. 11/28/2000 6,153,495 Kub et al. A73 6,154,475 11/28/2000 Soref et al. A74 12/12/2000 6,160,303 Fattaruso A75 6,162,688 12/19/2000 Gardner et al. A76 02/06/2001 6,184,111 Henley et al. A77 6,191,007 02/20/2001 Matsui et al. A78 6,191,432 02/20/2001 Sugiyama et al. A79 6,194,722 02/27/2001 Fiorini et al. A80 6,207,977 03/27/2001 Augusto A81 6,210,988 04/03/2001 Howe et al. A82 6,218,677 04/17/2001 Broekaert A83 05/15/2001 Fitzgerald et al. A84 6,232,138 6,235,567 05/22/2001 Huang A85 6,242,324 06/05/2001 Kub et al. A86 6,251,755 06/26/2001 Furukawa et al. A87 07/17/2001 6,261,929 Gehrke et al. A88 6,271,551 08/07/2001 Schmitz et al. A89 6,271,726 08/07/2001 Fransis et al. A90 6,291,321 09/18/2001 Fitzgerald A91 6,313,016 11/06/2001 Kibbel et al. A92 6,316,301 11/13/2001 Kant A93 6,323,108 11/27/2001 Kub et al. A94 **EXAMINER** DATE CONSIDERED



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U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A95	6,329,063	12/11/2001	Lo et al.			
	A96	6,335,546	01/01/2002	Tsuda et al.			
	A97	6,339,232	01/15/2002	Takagi			
	A98	6,350,993	02/26/2002	Chu et al.			
,*1.1	A99	6,368,733	04/09/2002	Nishinaga			
	A100	6,372,356	04/16/2002	Thornton et al.			
	A101	6,399,970	06/04/2002	Kubo et al.			
	A102	6,403,975	06/11/2002	Brunner et al.			
	A103	6,407,406	06/18/2002	Tezuka			
	A104	6,425,951	07/30/2002	Chu et al.			
	A105	6,429,061	08/06/2002	Rim			
	A106	6,521,041	02/18/2003	Wu et al.			
	A107	6,555,839	04/29/2003	Fitzgerald			
	A108	6,602,613	08/05/2003	Fitzgerald			01/17/2001
	A109	2001/0003364	06/14/2001	Sugawara et al.			
	A110	2002/0100942	08/01/2001	Fitzgerald et al.			
	A111	2002/0123197	09/05/2002	Fitzgerald et al.			
	A112	2002/0125471	09/12/2002	Fitzgerald et al.			
	A113	2002/0140031	10/03/2002	Rim			

FOREIGN PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
	BI	41 01 167	07/23/1992	DE				N	Abstract
	B2 /	0 514 018	11/19/1992	EP				N	Y
	B3/	0 587 520	03/16/1994	EP				N	Y

EXAMINER

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EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
	B4 /	0 683 522	11/22/1995	EP				N	Y
	B5	0 828 296	03/11/1998	EP				N	Y
	B6	0 829 908	03/18/1998	EP				N	Y
	B7	0 838 858	04/29/1998	EP				N	Abstract
	B8_	1 020 900	07/19/2000	EP				N	Y
	B9	1 174 928	01/23/2002	EP				N	Y
	B10	/ 2 342 777	04/19/2000	GB				Y	Y
	BII	5-166724	07/02/1993	JP				N	Abstract
	B12	-6-177046	06/24/1994	JP				N	Abstract
	B13	6-252046	09/09/1994	JP				Y	Y
	B14	· 7-94420 .	04/07/1995	JP				N	N
	B15_	×7-240372	09/12/1995	JP				N	Abstract
	B16	-10-270685	10/09/1998	JP				N	Y
	B17	2000-021783	01/21/2000	JP				N	Y
	B18	2000-031491	01/28/2000	JP				N	Y
	B19	~2001-319935	11/16/2001	JP				N	Y
	B20_	- 2002-076334	03/15/2002	JP				N	Y
	B21	2002-164520	06/07/2002	JP				N	Y
-	B22	2002-289533	10/04/2002	JP				N	Y
	B23_	98/59365	12/30/1998	WO				N	Y
	B24	-99/53539	10/21/1999	WO				N	Y
	B25	00/48239	08/17/2000	WO				N	Y
	B26	-00/54338	09/14/2000	WO				N	Y
	B27	01/022482	03/29/2001	WO				N	Y
	B28	01/54202	07/26/2001	WO				N	Y
	B29	-01/93338	12/06/2001	WO				N	Y



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	B30 0	1/99169	12/27/2001	WO				N	Y
		2/13262	02/14/2002	WO				N	Y
· ·	B32 02	2/15244	02/21/2002	wo				N	Y
	B33 . 02	2/27783	04/04/2002	WO				N	Y
	B34 02	2/47168	06/13/2002	wo				N	Y
	B35 02	2/071488	09/12/2002	WO				N	Y
	B36 02	2/071491	09/12/2002	wo				N	Y
	B37 02	2/071495	09/12/2002	wo				N	Y
	B38 -02	2/082514	10/17/2002	wo				N	Y
			OTHER A	RT, JOURN	NAL ART	ICLES, E	TC.	-	
EXAM. INIT.	OTHER	DOCUMENT	ΓS: (Including	g Author, Tit	le, Date, Re	levant Pag	es, Place of	Publication)	
	Tra	nsistors," <u>IED</u>	M Technical D	igest (1995 I	nternational	Electron De	evices Meet	de-Semiconduct ting), pp. 761-76	54.
	Ins	titute of Techn	ology, 1999, p	p. 1-154.				Thesis, Massac	
								Based Complem ruary 15, 1997),	
	cha	nnels for HMO	OS transistors,'	' Modern Phy	sics Letters	<u>B</u> , Vol. 15 ((2001), abst		
	the 199	1999 12th IEI 99), pp. 205-21	EE Internationa 10.	al Conference	on Micro El	lectro Mech	anical Syst	machining," Pro ems (MEMs) (Ja	anuary 17-21,
			Search for the 6 96), pp. 21.2.1		nel architectu	re for 0.18/	0.12 μm bu	ılk CMOS expei	rimental
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		OTHER ART, JOURN	JAL ARTICLES, ETC.	
EXAM. INIT.	ОТІ	HER DOCUMENTS: (Including Author, Tit	le, Date, Relevant Pages, Place of Publication)	
	C7 /	Bruel et al., "®SMART CUT: A Promising N International SOI Conference (October 1995)	New SOI Material Technology," Proceedings of the 1995 IEEE pp. 178-179.	
	C8 /	Bruel, "Silicon on Insulator Material Technol 1201-1202.	ogy," Electronic Letters, Vol. 13, No. 14 (July 6, 1995), pp.	
	C9	Bufler et al., "Hole transport in strained Si1-x Vol. 84, No. 10 (November 15, 1998), pp. 559	Gex alloys on Si1-yGey substrates," <u>Journal of Applied Physics</u> , 97-5602.	
	C10		apacitors in Standard Multilevel Interconnect Silicon ve Theory and Techniques, Vol. 44, No. 1 (January 1996), pp.	
	CII		le layer on an insulator in fabricating high-speed semiconductor ional Business Machines Corporation, USA (2002), abstract.	
	C12	Carlin et al., "High Efficiency GaAs-on-Si So 2000 (2000), pp. 1006-1011.	lar Cells with High Voc using Graded Gesi Buffers," IEEE –	
	C13	Chang et al., "Selective Etching of SiGe/Si Ho (January 1991), pp. 202-204.	eterostructures," <u>Journal of the Electrochemical Society</u> , No. 1	
	C14		t in Strained-Si n-MOSFETs Fabricated on SiGe-on-Insulator tters, Vol. 22, No. 7 (July 2001), pp. 321-323.	
	C15	, Cheng et al., "Relaxed Silicon-Germanium on Materials, Vol. 30, No. 12 (2001), pp. L37-L3	Insulator Substrate by Layer Transfer," <u>Journal of Electronic</u> 9.	
	C16		Ge epitaxial layers on Si and misfit dislocation interactions," A, Vol. 12, No. 4 (July/August 1994), pp. 1924-1931.	
	C17		tability of strained Si n- and p-MOSFETs on SiGe virtual echnology B, Vol. 19, No. 6 (Nov/Dec 2001), pp. 2268-2279.	
	C18		ion Densities in Ge on Si Using Graded SiGe Layers and ysics Letters, Vol. 72, Issue 14 (04/06/98), pp. 1718-1720.	
	C19 Eaglesham et al., "Dislocation-Free Stranski-Krastanow Growth of Ge on Si(100)," Physical Review Letters, Vol. 64, No. 16 (April 16, 1990), pp. 1943-1946.			
-	C20 Feijoo et al., "Epitaxial Si-Ge Etch Stop Layers with Ethylene Diamine Pyrocatechol for Bonded and Etchback Silicon-on-Insulator," Journal of Electronic Materials, Vol. 23, No. 6 (June 1994), pp. 493-496.			
	C21	Fischetti et al., "Band structure, deformation palloys," Journal of Applied Physics, Vol. 80, 1	potentials, and carrier mobility in strained Si, Ge, and SiGe No. 4 (August 15, 1996), pp. 2234-2252.	
	C22		n small Si devices. Part II. Effective electronmobility in thin-Vol. 89, No. 2 (January 15, 2001), pp. 1232-1250.	
EXAMIN	ER		DATE CONSIDERED	



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		OTHER ART, JOURN	JAL ARTICLES, ETC.		
EXAM. INIT.	ОТІ	HER DOCUMENTS: (Including Author, Tit	le, Date, Relevant Pages, Place of Publication)		
	C23	Fitzgerald et al., "Dislocation dynamics in rel Engineering, B67 (1999), pp. 53-61.	axed graded composition semiconductors," Materials Science and		
	C24		s for III-V integration with Si and high mobility two-dimensional nce Technology, B 10(4) (Jul/August 1992), pp. 1807-1819.		
	C25	Fitzgerald <i>et al.</i> , "Totally Relaxed GexSi1-x.L Substrates," <u>Applied Physics Letters</u> , Vol. 59,	ayers with Low Threading Dislocation Densities Grown on Si No. 7 (August 12, 1991), pp. 811-813.		
	C26	Garone et al., "Silicon vapor phase epitaxial g Letters, Vol. 56, No. 13 (March 26, 1990), pp	rowth catalysis by the presence of germane," <u>Applied Physics</u> . 1275-1277.		
	C27/	Gray et al., "Analysis and Design of Analog I	ntegrated Circuits," John Wiley & Sons, 1984, pp. 605-632.		
	C28		i heterostructures and its dependence on deposition technique ters, Vol. 63, No. 18 (November 1, 1993), pp. 2531-2533.		
	C29	Hackbarth et al., "Alternatives to thick MBE- (July 2000), pp. 148-151.	grown relaxed SiGe buffers," <u>Thin Solid Films</u> , Vol. 369, No. 1-2		
	C30	Hackbarth et al., "Strain relieved SiGe buffers Crystal Growth, Vol. 201/202 (1999), pp. 734	for Si-based heterostructure field-effect transistors," <u>Journal of</u> -738.		
	C31	Herzog et al., "SiGe-based FETs: buffer issue 41.	es and device results," Thin Solid Films, Vol. 380 (2000), pp. 36-		
	C32	Höck et al., "Carrier mobilities in modulation applications," Thin Solid Films, Vol. 336 (19)	doped Si1-xGex heterostructures with respect to FET 98), pp. 141-144.		
	C33	Höck <i>et al.</i> , "High hole mobility in Si0.17 Ge grown by plasma-enhanced chemical vapor de 2000), pp. 3920-3922.	0.83 channel metal-oxide-semiconductor field-effect transistors position," Applied Physics Letters, Vol. 76, No. 26 (June 26,		
	C34	Höck et al., "High performance 0.25 µm p-typ (September 17, 1998), pp. 1888-1889.	be Ge/SiGe MODFETs," <u>Electronics Letters</u> , Vol. 34, No. 19		
	C35	Huang et al., "High-quality strain-relaxed SiC Applied Physics Letters, Vol. 76, No. 19 (Magnetic Physics Letters)	e alloy grown on implanted silicon-on-insulator substrate," y 8, 2000), pp. 2680-2682.		
-	C36 Huang et al., "The Impact of Scaling Down to Deep Submicron on CMOS RF Circuits," IEEE Journal of Solid-State Circuits, Vol. 33, No. 7 (July 1998), pp. 1023-1036.				
	C37	Ishikawa et al., "Creation of Si-Ge-based SIM of the 1997 IEEE International SOI Conference	OX structures by low energy oxygen implantation," Proceedings to (October 1997), pp. 16-17.		
	C38	Ishikawa <i>et al.</i> , "SiGe-on-insulator substrate u 75, No. 7 (August 16, 1999), pp. 983-985.	sing SiGe alloy grown Si(001)," <u>Applied Physics Letters</u> , Vol.		
EXAMIN	ER		DATE CONSIDERED		



FORM PTO - 1449

INFORMATION DISCLOSURE STATEMENT

ATTORNEY DOCKET NO.: ASC-043C2

APPLICANT(S): Fitzgerald et al.

SERIAL NO.: 10/625,018

FILING DATE: July 23, 2003 GROUP: Not yet assigned

	OTHER ART, JOURNAL ARTICLES, ETC.						
EXAM. INIT.							
	C39	Ismail et al., "Modulation-doped n-type Si/SiGe with inverted interface," Applied Physics Letters, Vol. 65, No. 10 (September 5, 1994), pp. 1248-1250.					
	C40	/Ismail, "Si/SiGe High-Speed Field-Effect Transistors," Electron Devices Meeting, Washington, D.C. (December 10, 1995), pp. 20.1.1-20.1.4.					
	C41	Kearney et al., "The effect of alloy scattering on the mobility of holes in a Si1-xGex quantum well," Semiconductor Science and Technology, Vol. 13 (1998), pp. 174-180.					
	C42	Kim et al., "A Fully Integrated 1.9-GHz CMOS Low-Noise Amplifier," <u>IEEE Microwave and Guided Wave Letters</u> , Vol. 8, No. 8 (August 1998), pp. 293-295.					

- C43 Koester et al., "Extremely High Transconductance Ge/Si0.4Ge0.6 p-MODFET's Grown by UHV-CVD," IEEE Electron Device Letters, Vol. 21, No. 3 (March 2000), pp. 110-112.
 - König et al., "Design Rules for n-Type SiGe Hetero FETs," Solid State Electronics, Vol. 41, No. 10 (1997), pp. 1541-1547.
 - König et al., "p-Type Ge-Channel MODFET's with High Transconductance Grown on Si Substrates," IEEE Electron Device Letters, Vol. 14, No. 4 (April 1993), pp. 205-207.
 - C46 König et al., "SiGe HBTs and HFETs," Solid-State Electronics, Vol. 38, No. 9 (1995), pp. 1595-1602.
 - C47 Kummer *et al.*, "Low energy plasma enhanced chemical vapor deposition," <u>Materials Science and Engineering</u>, B89 (2002), pp. 288-295.
 - Kuznetsov *et al.*, "Technology for high-performance n-channel SiGe modulation-doped field-effect transistors," <u>Journal of Vacuum Science and Technology</u>, B 13(6) (November/December 1995), pp. 2892-2896.
 - C49 Larson, "Integrated Circuit Technology Options for RFIC's Present Status and Future Directions," <u>IEEE Journal of Solid-State Circuits</u>, Vol. 33, No. 3 (March 1998), pp. 387-399.
 - C50 Lee et al., "CMOS RF Integrated Circuits at 5 GHz and Beyond," Proceedings of the IEEE, Vol. 88, No. 10 (October 2000), pp. 1560-1571.
 - C51 Lee et al., "Strained Ge channel p-type metal-oxide-semiconductor field-effect transistors grown on Sil-xGex/Si virtual substrates," Applied Physics Letters, Vol. 79, No. 20 (November 12, 2001), pp. 3344-3346.

 C52 Lee et al., "Strained Ge channel p-type MOSFETs fabricated on Sil-xGex/Si virtual substrates," Materials
 - Research Society Symposium Proceedings, Vol. 686 (2002), pp. A1.9.1-A1.9.5.

 C53 Leitz et al., "Channel Engineering of SiGe-Based Heterostructures for High Mobility MOSFETs," Materials
 - Research Society Symposium Proceedings, Vol. 686 (2002), pp. A3.10.1-A3.10.6.

 C54 Leitz et al., "Dislocation glide and blocking kinetics in compositionally graded SiGe/Si," Journal of Applied Physics, Vol. 90, No. 6 (September 15, 2001), pp. 2730-2736.
 - C55 Leitz et al., "Hole mobility enhancements in strained Si/Si1-yGey p-type metal-oxide-semiconductor field-effect transistors grown on relaxed Si1-xGex (x<y) virtual substrates," Applied Physics Letters, Vol. 79, No. 25 (December 17, 2001), pp. 4246-4248.

EXAMINER

DATE CONSIDERED



INFORMATION DISCLOSURE STATEMENT APPL

ATTORNEY DOCKET NO.: ASC-043C2

APPLICANT(S): Fitzgerald et al.

	٠	FILING DATE: July 23, 2003 GROUP: Not yet assigned			
;	OTHER ART, JO	URNAL ARTICLES, ETC.			
EXAM. INIT.	OTHER DOCUMENTS: (Including Author	r, Title, Date, Relevant Pages, Place of Publication)			
		heterojunction complementary metal-oxide-semiconductor field effect fects," <u>Journal of Vacuum Science and Technology A</u> , Vol. 20, No.3			
	C57 Lu et al., "High Performance 0.1 μm Gat Transactions on Electron Devices, Vol. 4	te-Length P-Type SiGe MODFET's and MOS-MODFET's," <u>IEEE</u> 47, No. 8 (August 2000), pp. 1645-1652.			
	C58 Maiti <i>et al.</i> , "Strained-Si heterostructure Vol. 13 (1998), pp. 1225-1246.	field effect transistors," Semiconductor Science and Technology,			
	C59 Maszara, "Silicon-On-Insulator by Wafer (January 1991), pp. 341-347.	r Bonding: A Review," <u>Journal of the Electrochemical Society</u> , No. 1			
***************************************	C60 Meyerson et al., "Cooperative Growth Pl Physics Letters, Vol. 53, No. 25 (December 1997)	henomena in Silicon/Germanium Low-Temperature Epitaxy," <u>Applied</u> ber 19, 1988), pp. 2555-2557.			
		s with Strained-Si Channel for High Speed CMOS-Electron/Hole am on VLSI Technology, Honolulu (June 13-15), IEEE New York, pp.			
		ity Enhancement in Strained-Si MOSFET's on SiGe-on-Insulator ology," IEEE Electron Device Letters, Vol. 21, No. 5 (May 2000), pp.			
		ed-Si p-MOSFETs on SiGe-on-Insulator Substrates Fabricated by inical Digest (1999 International Electron Device Meeting), pp. 934-			
	C64 Nayak et al., "High-Mobility Strained-Si 10 (October 1996), pp. 1709-1716.	PMOSFET's," <u>IEEE Transactions on Electron Devices</u> , Vol. 43, No.			
	C65 O'Neill et al., "SiGe virtual substrate N-(Technology, Vol. 14 (1999), pp. 784-789	channel heterojunction MOSFETS," <u>Semiconductor Science and</u> 9.			
	C66 Papananos, "Radio-Frequency Microelec Academic Publishers, 1999, pp. 115-117	ctronic Circuits for Telecommunication Applications," Kluwer , 188-193.			
	C67 Parker et al., "SiGe heterostructure CMC pp. 1497-1506.	OS circuits and applications," <u>Solid State Electronics</u> , Vol. 43 (1999),			
	C68 Ransom et al., "Gate-Self-Aligned n-cha Electron Devices, Vol. 38, No. 12 (Dece	nnel and p-channel Germanium MOSFET's," <u>IEEE Transactions on</u> mber 1991), pp. 2695.			
	C69 Reinking et al., "Fabrication of high-mol Vol. 35, No. 6 (March 18, 1999), pp. 503	bility Ge p-channel MOSFETs on Si substrates," <u>Electronics Letters</u> , 3-504.			
	C70 Rim, "Application of Silicon-Based Heterostructures to Enhanced Mobility Metal-Oxide-Semiconductor Field Effect Transistors," PhD Thesis, Stanford University, 1999, pp. 1-184.				
- ,	C71 Rim et al., "Enhanced Hole Mobilities in 520.	Surface-Channel Strained-Si p-MOSFETs," <u>IEDM</u> (1995), pp. 517-			
	C72 Rim et al., "Fabrication and Analysis of Electron Devices, Vol. 47, No. 7 (July 20)	Deep Submicron Strained-Si N-MOSFET's," <u>IEEE Transactions on 000</u>), pp. 1406-1415.			
EXAMIN	ER	DATE CONSIDERED			



INFORMATION DISCLOSURE STATEMENT

FORM PTO – 1449

ATTORNEY DOCKET NO.: ASC-043C2

APPLICANT(S): Fitzgerald et al.

		SERIAL NO.: 10/625,018	
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	OTHER ART, J	OURNAL ARTICLES, ETC.	
EXAM. INIT.	OTHER DOCUMENTS: (Including Auth	nor, Title, Date, Relevant Pages, Place of Publication)	
	C73 Robbins et al., "A model for heterogeneous growth of Si1-xGex films for hydrides," Journal of Applied Physics, Vol. 69, No. 6 (March 15, 1991), pp. 3729-3732.		
	C74 Sadek et al., "Design of Si/SiGe Heterojunction Complementary Metal-Oxide-Semiconductor Tra		
	C75 Schäffler, "High-Mobility Si and Ge S 1515-1549.	tructures," Semiconductor Science and Technology, Vol. 12 (1997), pp.	
	C76 Sugimoto et al., "A 2V, 500 MHz and IEICE Trans Electron, Vol.E82-C, No	$3V$, 920 MHz Low-Power Current-Mode 0.6 μ m CMOS VCO Circuit," . 7 (July 1999), pp. 1327-1329.	
	C77 Ternent et al., "Metal Gate Strained Si 2000), pp. 38-43.	licon MOSFETs for Microwave Integrated Circuits," IEEE (October	
		composition of strained GeSi layers grown with disilane and germane," 20 (November 14, 1994), pp. 2579-2581.	
	C79 Usami et al., "Spectroscopic study of S Semiconductor Science and Technology	Si-based quantum wells with neighboring confinement structure," sy , (1997), abstract.	
		incement in Strained-Si N-Type Metal-Oxide-Semiconductor Field- vice Letters, Vol. 15, No. 3 (March 1994), pp. 100-102.	
		Hot-Electron Transfer in High Mobility, Strained-Si Multilayer igest (1993 International Electron Devices Meeting), pp. 545-548.	
		nsistors Fabricated in Strained Silicon/Relaxed Silicon-Germanium gest (1992 International Electron Devices Meeting), pp. 1000-1002.	
		Silicon/Relaxed Silicon Germanium Heterostructures to Metal-Oxides," PhD Thesis, Stanford University, 1994, pp. 1-205.	
	C84 Wolf <i>et al.</i> , "Silicon Processing for th CA, 1986, pp. 384-386.	e VLSI Era, Vol. 1: Process Technology," Lattice Press, Sunset Beach,	
		ughness: Dependence on Sign and Magnitude of Bulk Strain," <u>The</u> 22 (November 28, 1994), pp. 3006-3009.	
	C86 Xie et al., "Very High Mobility Two-Dimensional Hole Gas in Si/GexSi1-x/Ge Structures Grown by Molecular Beam Epitaxy," Applied Physics Letters, Vol. 63, Issue 16 (October 18, 1993), pp. 2263-2264. C87 Xie, "SiGe Field Effect Transistors," Materials Science and Engineering, Vol. 25 (1999), pp. 89-121.		
		y Silicon-on-Insulator P-MOSFET with a SiGe/Si Heterostructure rs, Vol. 21, No. 4 (April 2000), pp. 161-163.	
EXAMIN	ER	DATE CONSIDERED	



FORM PTO - 1449

INFORMATION DISCLOSURE STATEMENT

ATTORNEY DOCKET NO.: ASC-043C2

APPLICANT(S): Fitzgerald et al.

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FILING DATE: July 23, 2003 GROUP: Not yet assigned

OTHER ART, JOURNAL ARTICLES, ETC.			
OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)			
	Zhang et al., "Demonstration of a GaAs-Based Compliant Substrate Using Wafer Bonding and Substrate Removal Techniques," Electronic Materials and Processing Research Laboratory, Department of Electrical Engineering, University Park, PA 16802, 1998, pp. 25-28.		
C90	"Optimal Growth Technique and Structure for Strain Relaxation of Si-Ge Layers on Si Substrates," <u>IBM</u> <u>Technical Disclosure Bulletin</u> , Vol. 32, No. 8A (January 1990), pp. 330-331.		

"2 Bit/Cell EEPROM Cell Using Band to Band Tunneling for Data Read-Out," IBM Technical Disclosure

DATE CONSIDERED **EXAMINER**

Bulletin, Vol. 35, No. 4B (September 1992), pp. 136-140.

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